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May 6, 1999

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: ***60/084,063***
FILING DATE: ***May 4, 1998***

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PROVISIONAL APPLICATION FOR PATENT

Assistant Commissioner for Patents
Box Provisional Application
Washington, D. C. 20231

Sir:

This is a request for filing a **PROVISIONAL APPLICATION FOR PATENT** UNDER 37 CFR 1.53(b)(2).

INVENTOR(S)/APPLICANT(S)			
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TITLE OF THE INVENTION
METHOD AND APPARATUS FOR BAND EDGE TIMING RECOVERY OF DIGITAL VSB SIGNALS

In connection with this application, the following are enclosed:

3 Pages of Specification (Optional: ☐ Abstract ☐ Claims 0)

0 Sheets of Drawings

__ Assignment to: __

__ Statement of Small Entity Status

X Other: Return Postcard

Attorney Docket No. 023826/0115

The fee has been calculated as shown below. (Small entity fees indicated in parentheses.)

Filing Fee	$150 ($75)	$150.00
Rule 17(k) fee for non-English text	$130	0.00
Assignment Recording Fee	$ 40	0.00
	TOTAL FEE	$150.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No ☐ Yes, the name of the U.S. Government agency and the Government contract number are: .

A check in the amount of the above TOTAL FEE is attached. The Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741.

Respectfully submitted,

Date: May 4, 1998
Docket No.: 023826/0115

Bernhard D. Saxe
Registration No. 28,665

Method and Apparatus for Band Edge Timing Recovery of Digital VSB Signals

1. Summary of the Invention

Sampling phase has a major impact on the performance of a digital modem receiver. Common digital VSB receivers uses known sync pattern to extract sampling timing information [1,2].
The suggested timing recovery approach utilizes fast "blind" algorithm, that is based on maximization of the energy contained in the sampled received signal. The suggested algorithm is more robust to signal reflections in the channel, and has acquisition time faster than prior art receiver that utilize sync patterns to extract timing information.

2. Background

Prior art VSB receivers utilize known sync pattern to extract timing information. For example, the digital VSB ATSC A/55 standard defines 4 symbols sync pattern every 834 symbols. Zenith's receiver [2] uses that pattern to exract the timing phase. The main disadvantages of such timing block are:
(1) long convergence time
(2) converges to a poor solution in a presence of strong and close (less than pattern length) inter symbol interference.

3. The Disclosed Invention

The disclosed invention is a method for timing recovery of digital VSB signals using non-linear transformation of band edge filtering, and maximization of the energy contained in the sampled received pulse.
A block diagram of the algorithm is shown in Fig. 1.

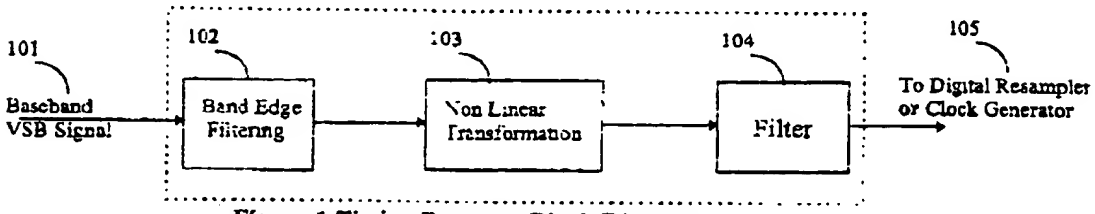

Figure 1 Timing Recovery Block Diagram

The baseband VSB signal **101** is filtered by band-edge filter **102**. The filter's output is fed to a non linear transformer **103**, which its output is filtered by linear filter **104**.

The output of the timing recovery block **105** is used as a timing correction signal to a digital resampler unit or to an external clock source (VCXO).

4. Preferred Embodiment

The following section describes the preferred embodiment of the suggested algorithm.

A general block diagram of VSB receiver is shown in Fig.2.

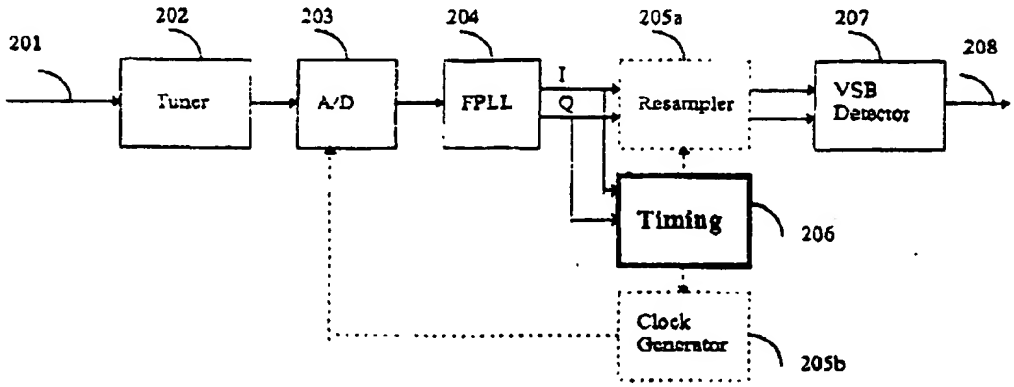

Figure 2 General Block Diagram of a VSB Receiver

The antenna output signal **201** is down converted to a IF frequency by the tuner **202**. The A/D **203** is sampling the signal for further processing. The FPLL **204** is using the pilot tone of a digital VSB signal to lock the carrier frequency and phase. The output from the FPLL **204** which is usually an *I/Q* signal, is fed to the timing recovery block **206**. The timing correction signal is used by the digital resampler unit **205a** or external clock generator **205b**. The input to the VSB detector **207** is a T-spaced or fractionally sampled signal which is synchronized with the symbol clock of the signal. The output of the VSB detector **207** is the detected data.
The preferred embodiment of the timing recovery block **206** is described as follows:

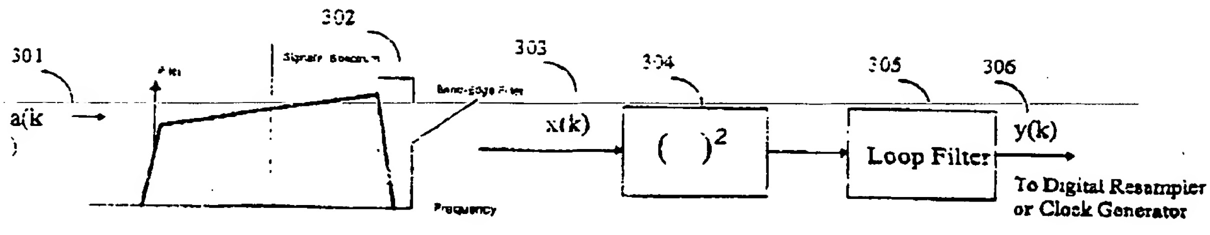

Figure 3 The preferred embodiment for the suggested algorithm.

The input signal to the timing recovery block a(k) **301** is filtered by narrow band-pass filter centered at the signal edge **302**. The filter's output x(k) **303** is passed through a non-linear transformation which is simply a square function **304**. The loop filter **305** can be described by the following equations:

$$y(k) = d \cdot x^2(k) + g(k)$$
$$g(k) = g(k-1) + c \cdot x^2(k-1)$$

where x(k) is the filter's input **303**, *c* and *d* are constants, and y(k) **306** is the filter's output.

References

[1] ATSC Digital Television Standard Doc. A/55
[2] "*Receiver Post Coder Selection Circuit*", US patent no. 5,260,793, Nov. 9, 1993.